## TRANSMITTAL

Electronic Version v1.1

Stylesheet Version v1.1.0

Title of Invention

A SYSTEM AND METHOD OF PROVIDING ERROR DETECTION AND CORRECTION CAPABILITY IN AN INTEGRATED CIRCUIT USING REDUNDANT LOGIC CELLS OF AN EMBEDDED FPGA

Application Number:

Date:

First Named Applicant:

JOHN M. COHN

Confirmation Number:

Attorney Docket Number: BUR920040001US1

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Submitted By:	Elec. Sign.	Sign. Capacity
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Documents being submitted:	Files	
us-fee-sheet	BUR920040001US1-usfees.xml	
	us-fee-sheet.xsl	
	us-fee-sheet.dtd	
us-assignment	BUR920040001US1-usassn.xml	
	us-assignment.xsl	
	us-assignment.dtd	
	BUR920040001US1Assign1.tif	
	BUR920040001US1Assign2.tif	
us-request	BUR920040001US1-usrequ.xml	
	us-request.dtd	
	us-request.xsl	
application-body	BUR920040001US1SPEC-trans.xml	
	us-application-body.xsl	
	application-body.dtd	
	wipo.ent	
	mathml2.dtd	
	mathml2-qname-1.mod	
	isoamsa.ent	
	isoamsb.ent	
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	isoamsn.ent	
	isoamso.ent	
	isoamsr.ent	
	isogrk3.ent	
	isomfrk.ent	
	isomopf.ent	
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	isotech.ent	
	isobox.ent	
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	isocyr2.ent	
	isodia.ent	
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	isolat2.ent	
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	isopub.ent	
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	mmlalias.ent	
	soextblx.dtd	
	BUR920040001US1Fig1.tif	
	BUR920040001US1Fig2.tif	
	BUR920040001US1Fig3.tif	
us-declaration	BUR920040001US1Dec1.tif	
us-declaration	BUR920040001US1Dec2.tif	
Comments		

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